



## QUAD CHANNEL HIGH SIDE SOLID STATE RELAY

| TYPE   | R <sub>DS(on)</sub> (*) | I <sub>lim</sub> | V <sub>CC</sub> |
|--------|-------------------------|------------------|-----------------|
| VNQ600 | 35mΩ                    | 25A              | 36 V            |

(\*) Per each channel

- DC SHORT CIRCUIT CURRENT: 25A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE & OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
  - LOSS OF GROUND & LOSS OF V<sub>CC</sub>
- REVERSE BATTERY PROTECTION (\*\*)

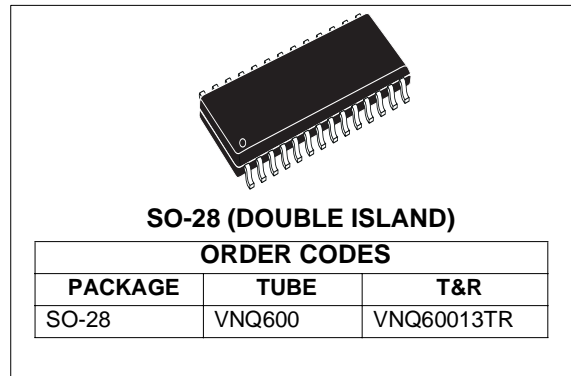
### DESCRIPTION

The VNQ600 is a quad HSD formed by assembling two VND600 chips in the same SO-28

### ABSOLUTE MAXIMUM RATING

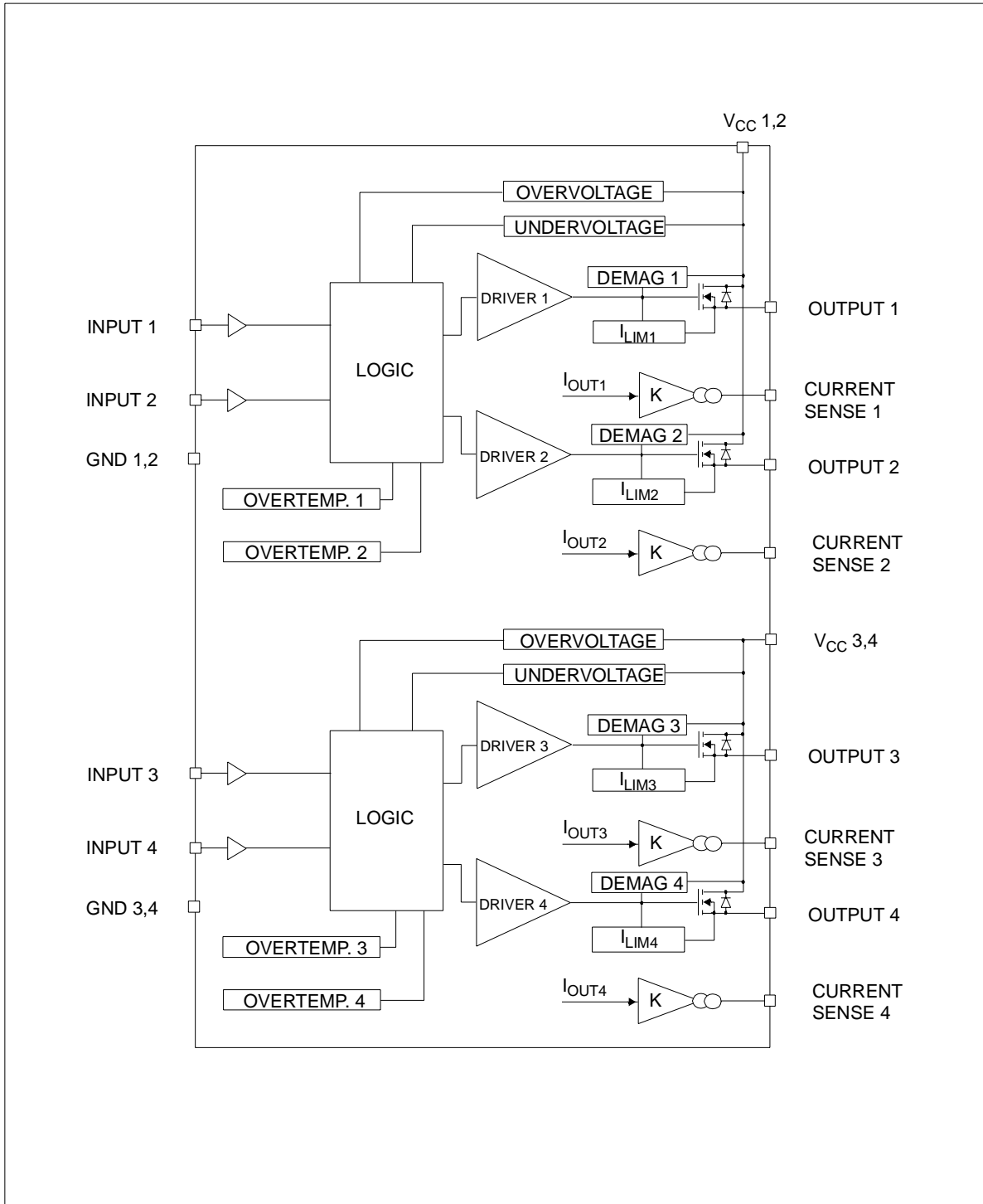
| Symbol               | Parameter  | Value              | Unit   |
|----------------------|--|--------------------|--------|
| V <sub>CC</sub>      | Supply voltage (continuous)  | 41                 | V      |
| -V <sub>CC</sub>     | Reverse supply voltage (continuous)  | -0.3               | V      |
| I <sub>OUT</sub>     | Output current (continuous), for each channel  | 15                 | A      |
| I <sub>R</sub>       | Reverse output current (continuous), for each channel  | -15                | A      |
| I <sub>IN</sub>      | Input current  | +/- 10             | mA     |
| V <sub>CSSENSE</sub> | Current sense maximum voltage  | -3<br>+15          | V<br>V |
| I <sub>GND</sub>     | Ground current at T <sub>pins</sub> ≤ 25°C (continuous)  | -200               | mA     |
| V <sub>ESD</sub>     | Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)   |                    |        |
|                      | - INPUT  | 4000               | V      |
|                      | - CURRENT SENSE  | 2000               | V      |
|                      | - OUTPUT   | 5000               | V      |
|                      | - V <sub>CC</sub>  | 5000               | V      |
| E <sub>MAX</sub>     | Maximum Switching Energy<br>(L=0.11mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =40A) | 126                | mJ     |
| P <sub>tot</sub>     | Power dissipation (per island) at T <sub>lead</sub> =25°C  | 6.25               | W      |
| T <sub>j</sub>       | Junction operating temperature   | Internally Limited | °C     |
| T <sub>stg</sub>     | Storage temperature  | -55 to 150         | °C     |

(\*\*) See application schematic at page 9.

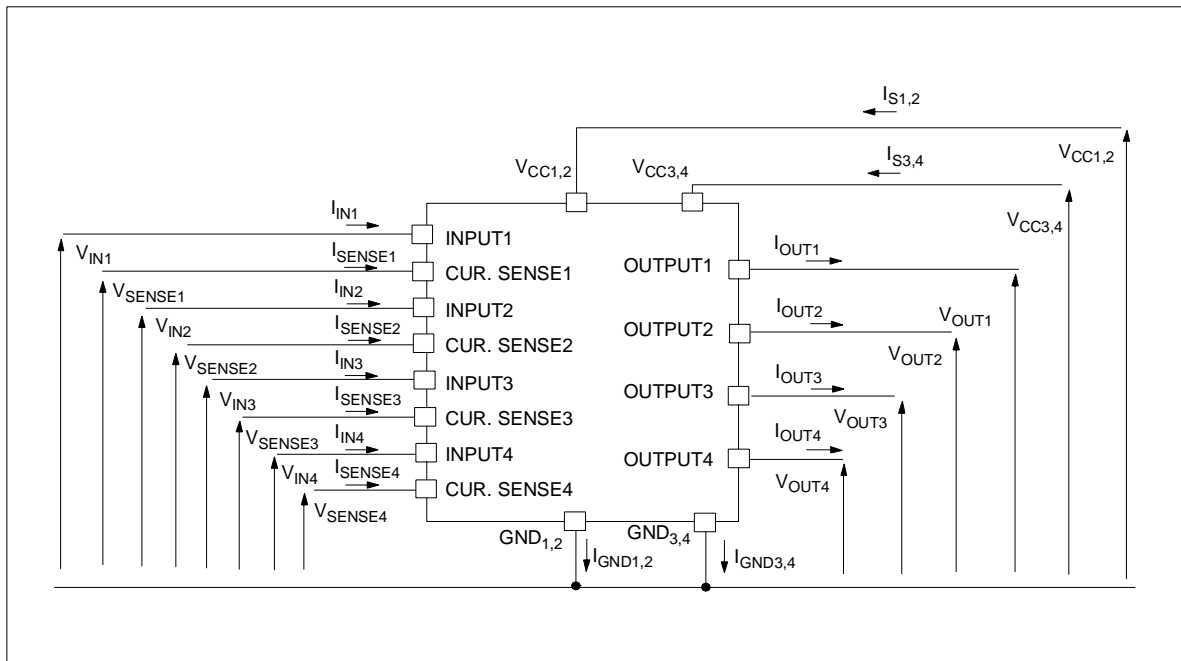


package. The VND600 is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ600 is intended for driving any type of multiple loads with one side connected to ground. This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents. Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

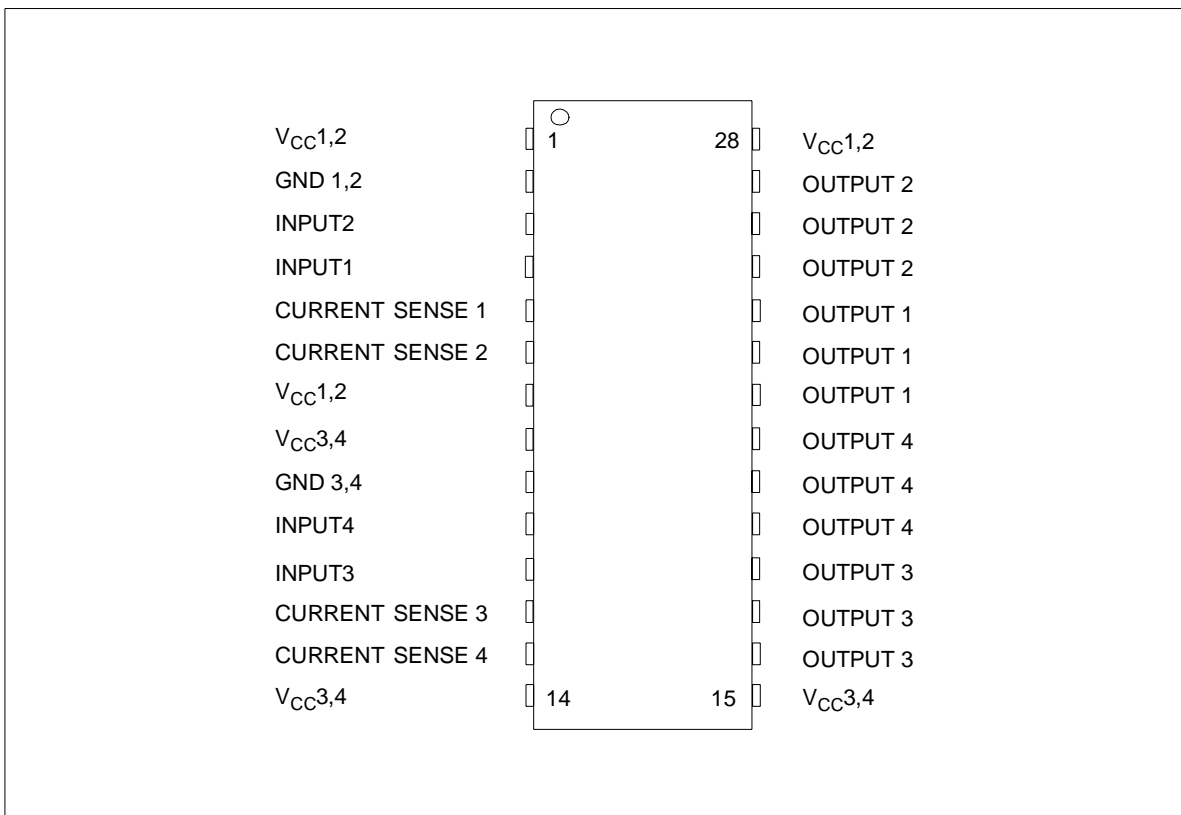
BLOCK DIAGRAM



**CURRENT AND VOLTAGE CONVENTIONS**



**CONNECTION DIAGRAM (TOP VIEW)**



## THERMAL DATA (Per island)

| Symbol         | Parameter  | Value  | Unit |
|----------------|--|--------|------|
| $R_{thj-lead}$ | Thermal resistance Junction-lead                   | 20     | °C/W |
| $R_{thj-amb}$  | Thermal resistance Junction-ambient (one chip ON)  | 60 (*) | °C/W |
| $R_{thj-amb}$  | Thermal Resistance Junction-ambient (two chips ON) | 46 (*) | °C/W |

(\*) When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins.  
Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified)

(Per each channel)

## POWER

| Symbol                | Parameter                | Test Conditions   | Min | Typ | Max | Unit |
|-----------------------|--------------------------|---|-----|-----|-----|------|
| V <sub>CC</sub> (**)  | Operating supply voltage |   | 5.5 | 13  | 36  | V    |
| V <sub>USD</sub> (**) | Undervoltage shut-down   |   | 3   | 4   | 5.5 | V    |
| V <sub>OV</sub> (**)  | Overvoltage shut-down    |   | 36  |     |     | V    |
| R <sub>ON</sub>       | On state resistance      | I <sub>OUT</sub> 1,2,3,4=5A; T <sub>j</sub> =25°C   |     |     | 35  | mΩ   |
|                       |                          | I <sub>OUT</sub> 1,2,3,4=5A; T <sub>j</sub> =150°C  |     |     | 70  | mΩ   |
|                       |                          | I <sub>OUT</sub> 1,2,3,4=3A; V <sub>CC</sub> =6V  |     |     | 120 | mΩ   |
| V <sub>clamp</sub>    | Clamp Voltage            | I <sub>CC</sub> =20mA (see note 1)  | 41  | 48  | 55  | V    |
| I <sub>S</sub> (**)   | Supply current           | Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V                                  |     | 12  | 40  | µA   |
|                       |                          | Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V;<br>T <sub>j</sub> =25°C         |     | 12  | 25  | µA   |
|                       |                          | On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V;<br>I <sub>OUT</sub> =0A; R <sub>SENSE</sub> =3.9KΩ |     |     | 6   | mA   |
| I <sub>L(off1)</sub>  | Off state output current | V <sub>IN</sub> =V <sub>OUT</sub> =0V   | 0   |     | 50  | µA   |
| I <sub>L(off2)</sub>  | Off State Output Current | V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V   | -75 |     | 0   | µA   |
| I <sub>L(off3)</sub>  | Off State Output Current | V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C                      |     |     | 5   | µA   |
| I <sub>L(off4)</sub>  | Off State Output Current | V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C                       |     |     | 3   | µA   |

SWITCHING (V<sub>CC</sub>=13V)

| Symbol                                 | Parameter              | Test Conditions                                    | Min | Typ                  | Max | Unit |
|--|------------------------|--|-----|----------------------|-----|------|
| t <sub>d(on)</sub>                     | Turn-on delay time     | R <sub>L</sub> =2.6Ω channels 1,2,3,4 (see fig. 1) |     | 40                   |     | µs   |
| t <sub>d(off)</sub>                    | Turn-off delay time    | R <sub>L</sub> =2.6Ω channels 1,2,3,4 (see fig. 1) |     | 40                   |     | µs   |
| (dV <sub>OUT</sub> /dt) <sub>on</sub>  | Turn-on voltage slope  | R <sub>L</sub> =2.6Ω channels 1,2,3,4 (see fig. 1) |     | See relative diagram |     | V/µs |
| (dV <sub>OUT</sub> /dt) <sub>off</sub> | Turn-off voltage slope | R <sub>L</sub> =2.6Ω channels 1,2,3,4 (see fig. 1) |     | See relative diagram |     | V/µs |

## PROTECTIONS

| Symbol             | Parameter                      | Test Conditions   | Min                 | Typ                 | Max                 | Unit |
|--------------------|--------------------------------|---|---------------------|---------------------|---------------------|------|
| I <sub>lim</sub>   | DC Short circuit current       | V <sub>CC</sub> =13V                                    | 25                  | 40                  | 70                  | A    |
|                    |                                | 5.5V < V <sub>CC</sub> < 36V                            |                     |                     | 70                  | A    |
| T <sub>TSD</sub>   | Thermal shut-down temperature  |   | 150                 | 175                 | 200                 | °C   |
| T <sub>R</sub>     | Thermal reset temperature      |   | 135                 |                     |                     | °C   |
| T <sub>hyst</sub>  | Thermal hysteresis             |   | 7                   | 15                  |                     | °C   |
| V <sub>demag</sub> | Turn-off output voltage clamp  | I <sub>OUT</sub> =2A; L=6mH                             | V <sub>CC</sub> -41 | V <sub>CC</sub> -48 | V <sub>CC</sub> -55 | V    |
| V <sub>ON</sub>    | Output voltage drop limitation | I <sub>OUT</sub> =0.5A; T <sub>j</sub> = -40°C...+150°C |                     | 50                  |                     | mV   |

(\*\*) Per island

CURRENT SENSE ( $9V < V_{CC} < 16V$ ) (See Fig. 3)

| Symbol         | Parameter  | Test Conditions   | Min          | Typ          | Max          | Unit     |
|----------------|--|---|--------------|--------------|--------------|----------|
| $K_1$          | $I_{OUT}/I_{SENSE}$  | $I_{OUT1,2}=0.35A$ ; $V_{SENSE}=0.5V$ ;<br>$T_j = -40^{\circ}C...+150^{\circ}C$                                   | 3300         | 4350         | 6000         |          |
| $dK_1/K_1$     | Current Sense Ratio Drift  | $I_{OUT1}$ or $I_{OUT2}=0.5A$ ;<br>$V_{SENSE}=0.5V$ ; other channels<br>open; $T_j = -40^{\circ}C...150^{\circ}C$ | -10          |              | +10          | %        |
| $K_2$          | $I_{OUT}/I_{SENSE}$  | $I_{OUT}=2A$ ; $V_{SENSE}=2.5V$ ; $T_j=-40^{\circ}C$<br>$T_j = 25^{\circ}C...+150^{\circ}C$                       | 3900<br>4150 | 4850<br>4850 | 6000<br>5800 |          |
| $dK_2/K_2$     | Current Sense Ratio Drift  | $I_{OUT1}$ or $I_{OUT2}=5A$ ; $V_{SENSE}=4V$ ;<br>other channels open;<br>$T_j=-40^{\circ}C...150^{\circ}C$       | -6           |              | +6           | %        |
| $K_3$          | $I_{OUT}/I_{SENSE}$  | $I_{OUT}=4A$ ; $V_{SENSE}=4V$ ; $T_j=-40^{\circ}C$<br>$T_j = 25^{\circ}C...+150^{\circ}C$                         | 4150<br>4400 | 4900<br>4900 | 6000<br>5750 |          |
| $dK_3/K_3$     | Current Sense Ratio Drift  | $I_{OUT1}$ or $I_{OUT2}=15A$ ; $V_{SENSE}=4V$ ;<br>other channels open;<br>$T_j=-40^{\circ}C...150^{\circ}C$      | -6           |              | +6           | %        |
| $V_{SENSE1,2}$ | Max analog sense output<br>voltage                               | $V_{CC}=5.5V$ ; $I_{OUT1,2}=2A$ ;<br>$R_{SENSE}=10K\Omega$  | 2            |              |              | V        |
|                |  | $V_{CC}>8V$ ; $I_{OUT1,2}=4A$ ;<br>$R_{SENSE}=10K\Omega$  | 4            |              |              | V        |
| $V_{SENSEH}$   | Analog sense output voltage in<br>overtemperature condition      | $V_{CC}=13V$ ; $R_{SENSE}=3.9K\Omega$   |              | 5            |              | V        |
| $R_{VSENSEH}$  | Analog Sense Output<br>Impedance in<br>Overtemperature Condition | $V_{CC}=13V$ ; $T_j>T_{TSD}$ ; All channels<br>open   |              | 400          |              | $\Omega$ |
| $t_{DSENSE}$   | Current sense delay response                                     | to 90% $I_{SENSE}$ (see note 2)   |              |              | 500          | $\mu s$  |

## LOGIC INPUT

| Symbol        | Parameter                | Test Conditions | Min  | Typ  | Max  | Unit    |
|---------------|--------------------------|-----------------|------|------|------|---------|
| $V_{IL}$      | Low level input voltage  |                 |      |      | 1.25 | V       |
| $V_{IH}$      | High level input voltage |                 | 3.25 |      |      | V       |
| $V_{I(hyst)}$ | Input hysteresis voltage |                 | 0.5  |      |      | V       |
| $I_{IL}$      | Input current            | $V_{IN}=1.5V$   | 1    |      |      | $\mu A$ |
| $I_{IN}$      | Input current            | $V_{IN}=3.5V$   |      |      | 10   | $\mu A$ |
| $V_{ICL}$     | Input clamp voltage      | $I_{IN}=1mA$    | 6    | 6.8  | 8    | V       |
|               |                          | $I_{IN}=-1mA$   |      | -0.7 |      | V       |

Note 1:  $V_{clamp}$  and  $V_{OV}$  are correlated. Typical difference is 5V.

Note 2: current sense signal delay after positive input slope.

Note: Sense pin doesn't have to be left floating.

TRUTH TABLE (per channel)

| CONDITIONS                    | INPUT | OUTPUT | SENSE                          |
|-------------------------------|-------|--------|--------------------------------|
| Normal operation              | L     | L      | 0                              |
|                               | H     | H      | Nominal                        |
| Overtemperature               | L     | L      | 0                              |
|                               | H     | L      | $V_{SENSEH}$                   |
| Undervoltage                  | L     | L      | 0                              |
|                               | H     | L      | 0                              |
| Overvoltage                   | L     | L      | 0                              |
|                               | H     | L      | 0                              |
| Short circuit to GND          | L     | L      | 0                              |
|                               | H     | L      | $(T_j < T_{TSD})$ 0            |
|                               | H     | L      | $(T_j > T_{TSD})$ $V_{SENSEH}$ |
| Short circuit to $V_{CC}$     | L     | H      | 0                              |
|                               | H     | H      | < Nominal                      |
| Negative output voltage clamp | L     | L      | 0                              |

**ELECTRICAL TRANSIENT REQUIREMENTS**

| ISO T/R<br>7637/1<br>Test Pulse | Test Levels<br>I | Test Levels<br>II | Test Levels<br>III | Test Levels<br>IV | Test Levels<br>Delays and Impedance |
|---------------------------------|------------------|-------------------|--------------------|-------------------|-------------------------------------|
| 1                               | -25V             | -50V              | -75V               | -100V             | 2ms, 10Ω                            |
| 2                               | +25V             | +50V              | +75V               | +100V             | 0.2ms, 10Ω                          |
| 3a                              | -25V             | -50V              | -100V              | -150V             | 0.1μs, 50Ω                          |
| 3b                              | +25V             | +50V              | +75V               | +100V             | 0.1μs, 50Ω                          |
| 4                               | -4V              | -5V               | -6V                | -7V               | 100ms, 0.01Ω                        |
| 5                               | +26.5V           | +46.5V            | +66.5V             | +86.5V            | 400ms, 2Ω                           |

| ISO T/R<br>7637/1<br>Test Pulse | Test Levels Result<br>I | Test Levels Result<br>II | Test Levels Result<br>III | Test Levels Result<br>IV |
|---------------------------------|-------------------------|--------------------------|---------------------------|--------------------------|
| 1                               | C                       | C                        | C                         | C                        |
| 2                               | C                       | C                        | C                         | C                        |
| 3a                              | C                       | C                        | C                         | C                        |
| 3b                              | C                       | C                        | C                         | C                        |
| 4                               | C                       | C                        | C                         | C                        |
| 5                               | C                       | E                        | E                         | E                        |

| Class | Contents   |
|-------|--|
| C     | All functions of the device are performed as designed after exposure to disturbance.   |
| E     | One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device. |

**Figure 1: Switching Characteristics (Resistive load  $R_L=2.6\Omega$ )**

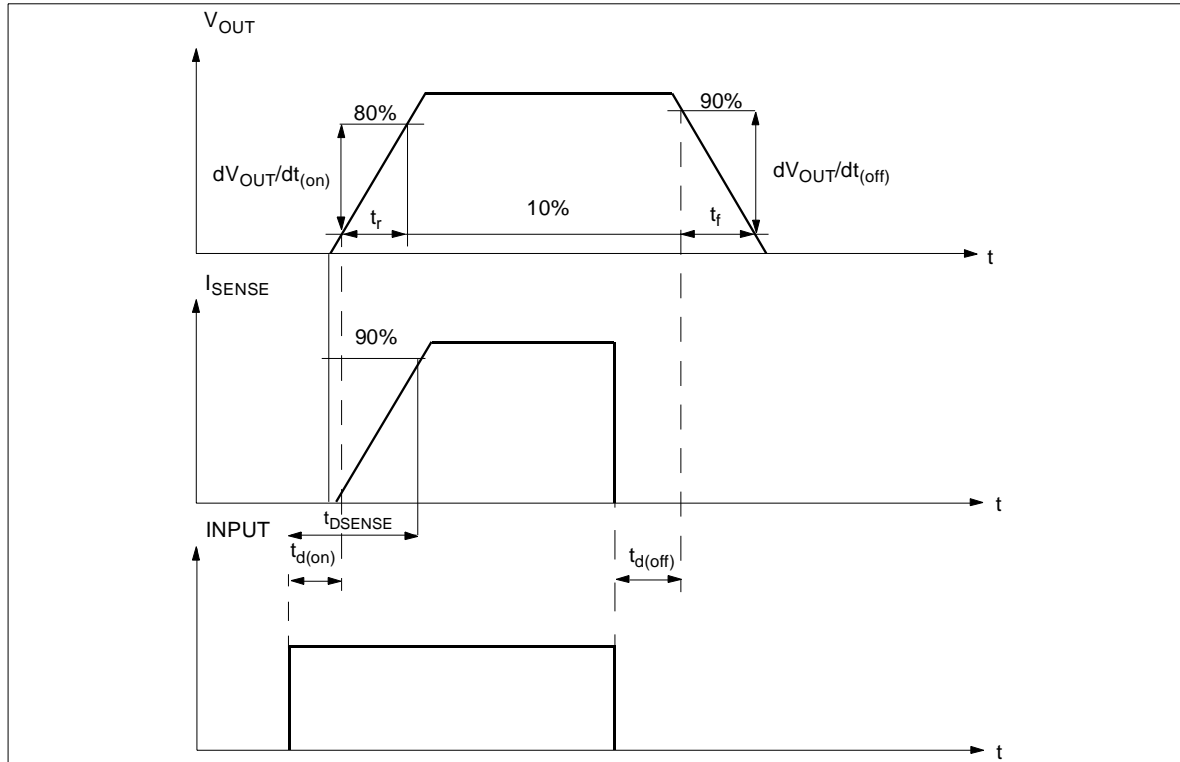
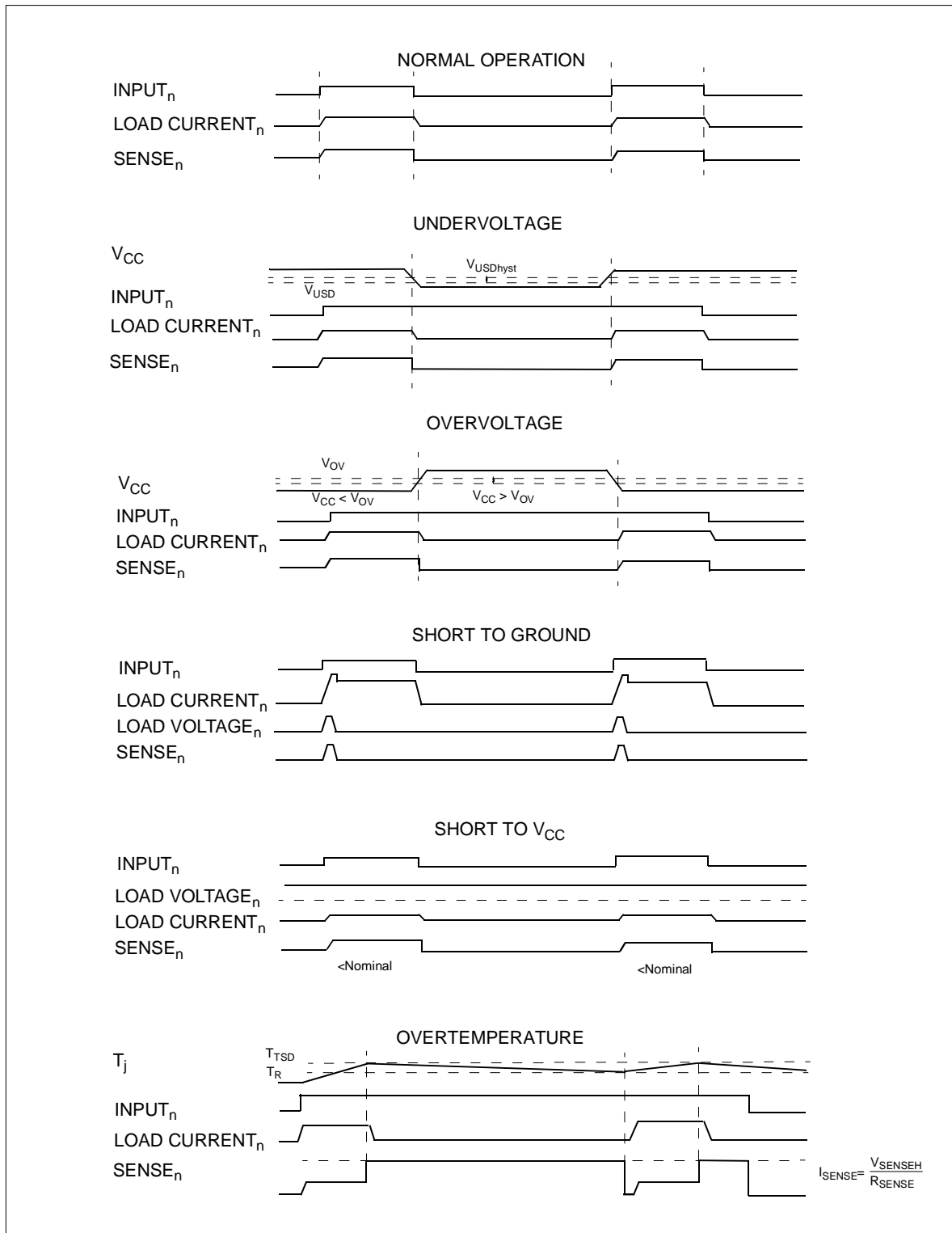
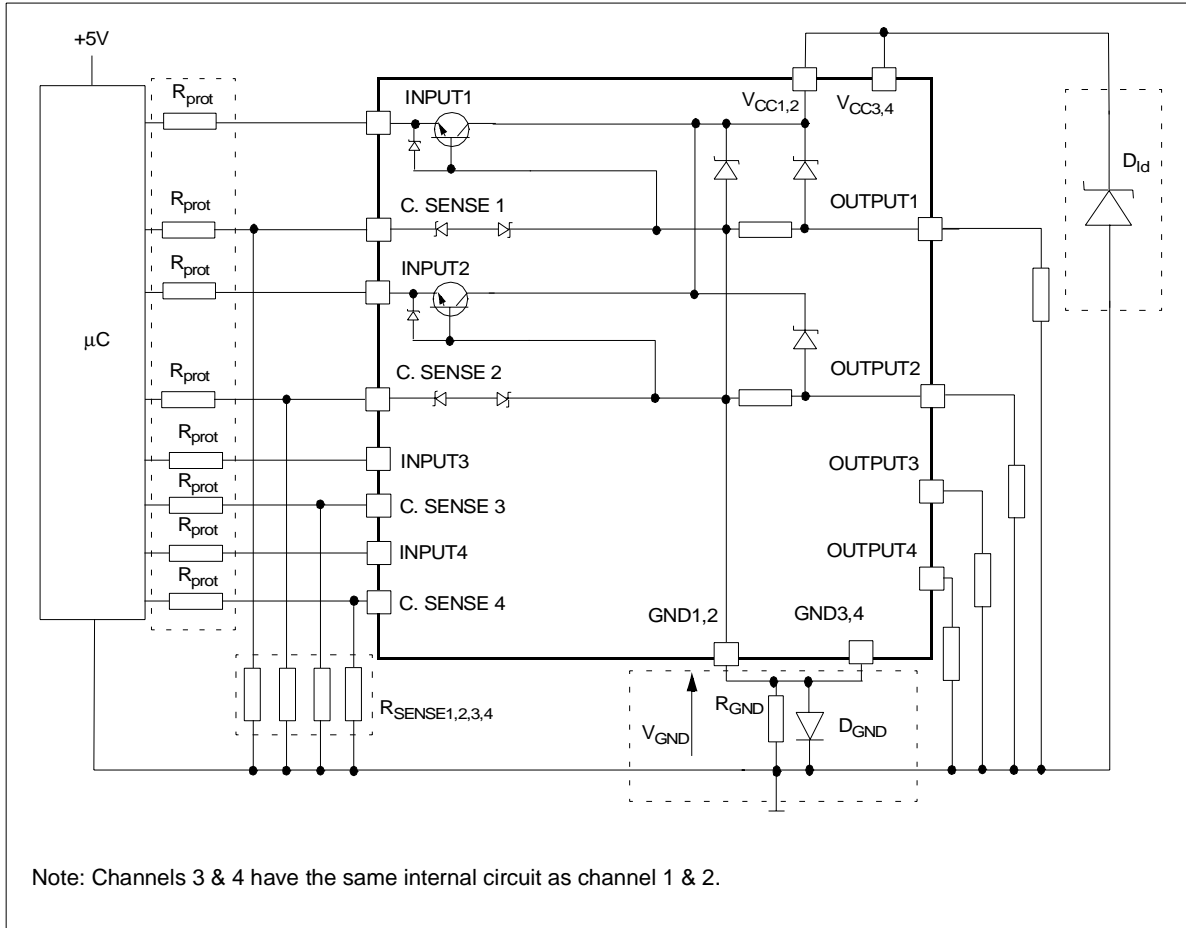


Figure 2: Waveforms (per each chip)





APPLICATION SCHEMATIC



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600mV / 2(I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds

and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

**LOAD DUMP PROTECTION**

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

**μC I/Os PROTECTION:**

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

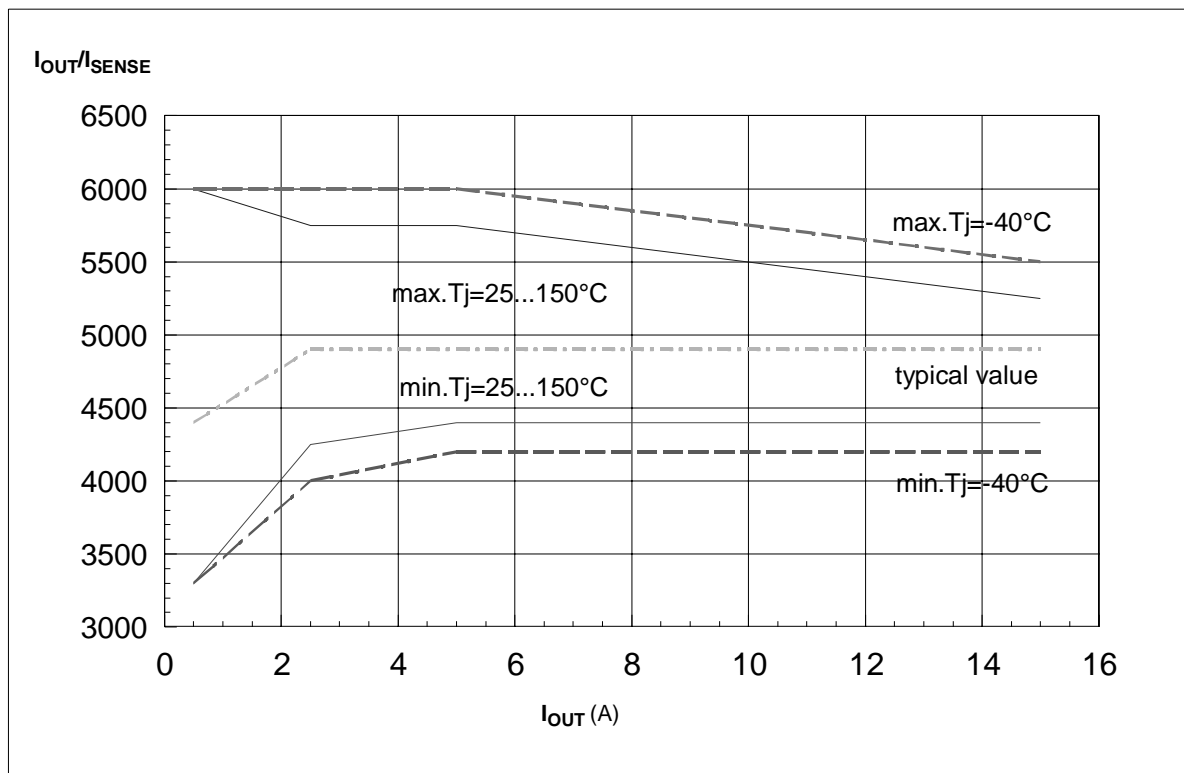
$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

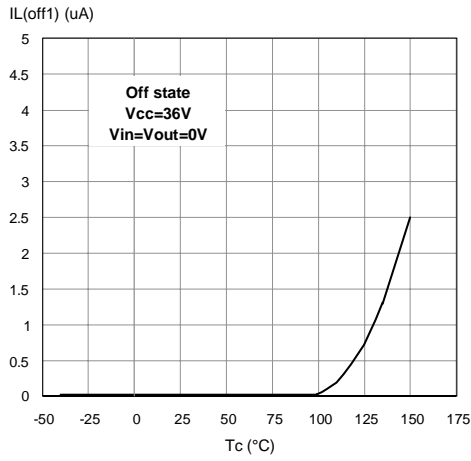
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$   
 $5k\Omega \leq R_{prot} \leq 65k\Omega$ .

Recommended  $R_{prot}$  value is 10kΩ.

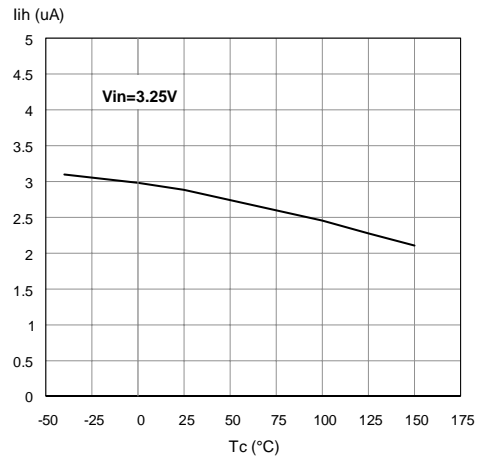
**Figure 3:**  $I_{OUT}/I_{SENSE}$  versus  $I_{OUT}$



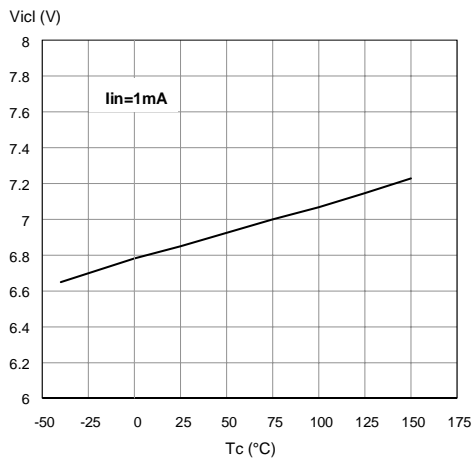
Off State Output Current



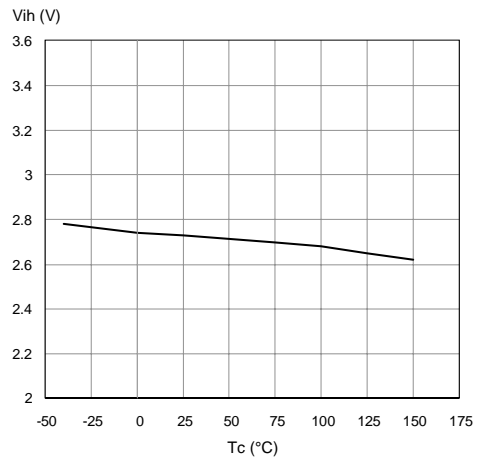
High Level Input Current



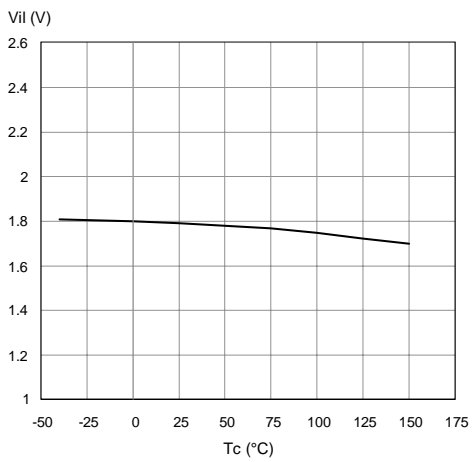
Input Clamp Voltage



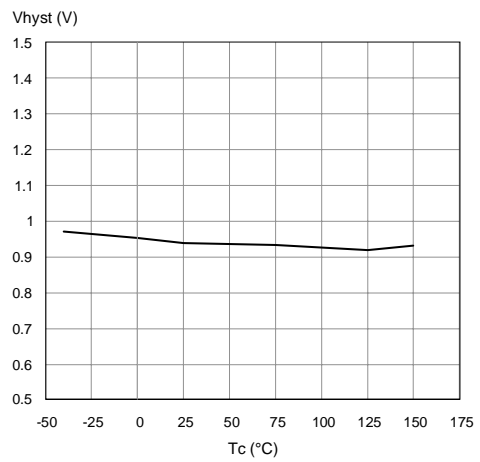
Input High Level



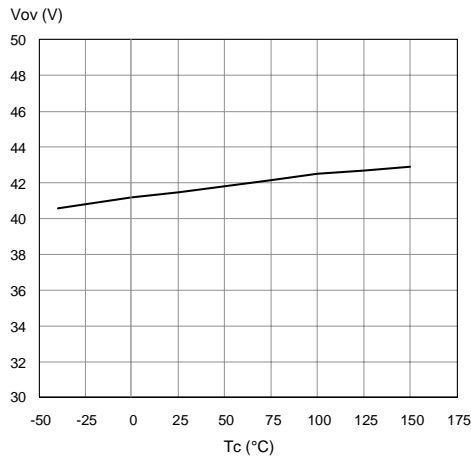
Input Low Level



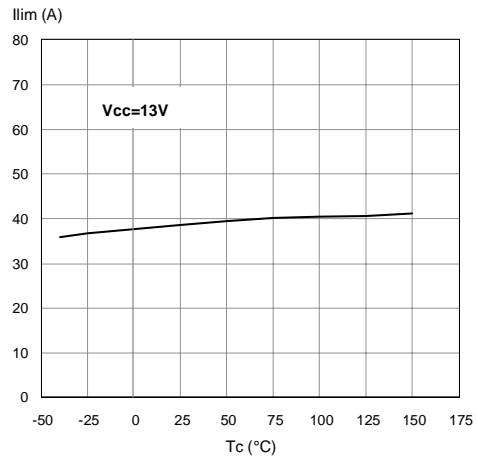
Input Hysteresis Voltage



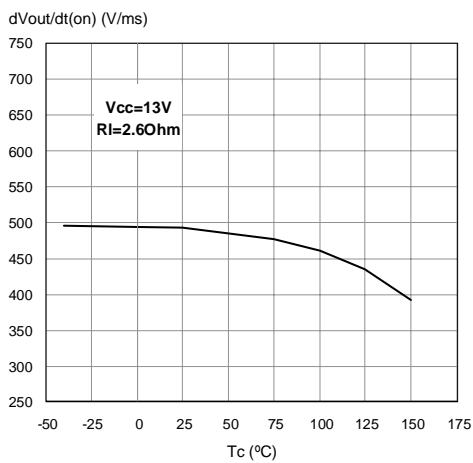
Overvoltage Shutdown



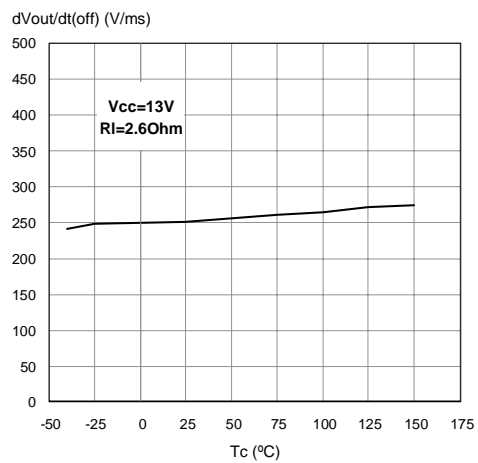
I<sub>LIM</sub> Vs T<sub>case</sub>



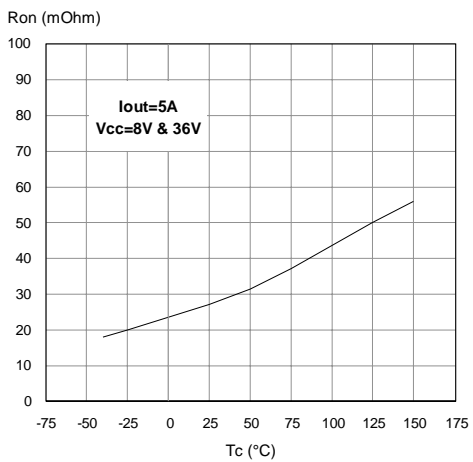
Turn-on Voltage Slope



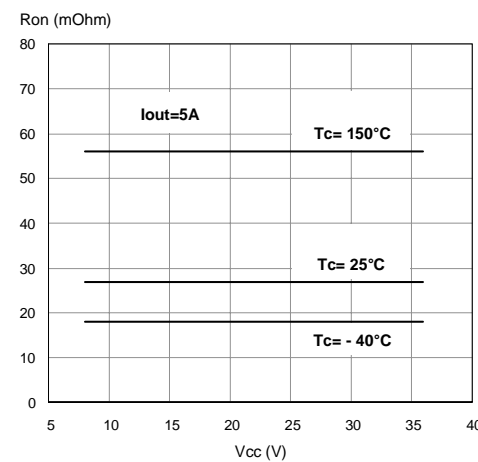
Turn-off Voltage Slope



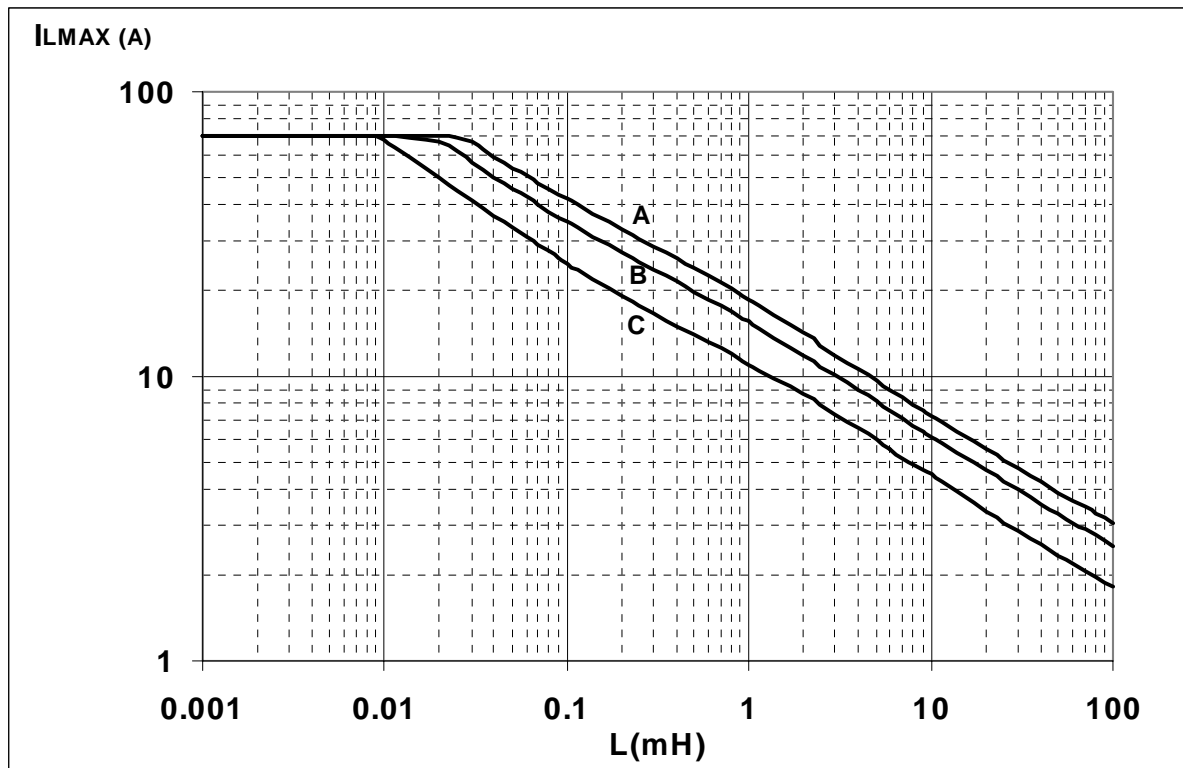
On State Resistance Vs T<sub>case</sub>



On State Resistance Vs V<sub>CC</sub>



## Maximum turn off current versus load inductance



A = Single Pulse at  $T_{jstart}=150^{\circ}\text{C}$

B = Repetitive pulse at  $T_{jstart}=100^{\circ}\text{C}$

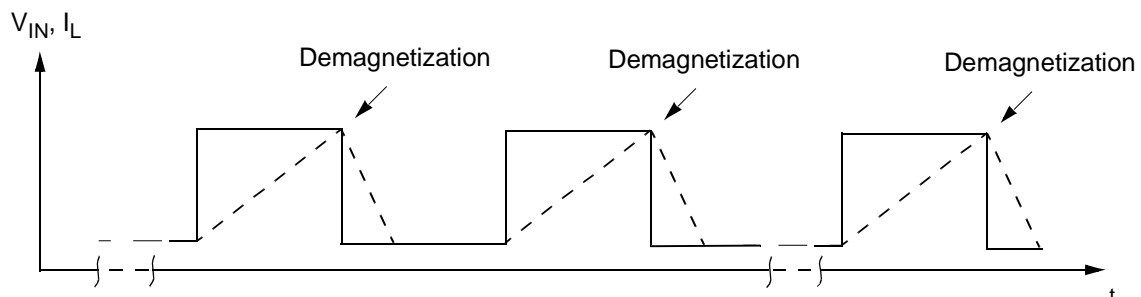
C = Repetitive Pulse at  $T_{jstart}=125^{\circ}\text{C}$

Conditions:

$V_{CC}=13.5\text{V}$

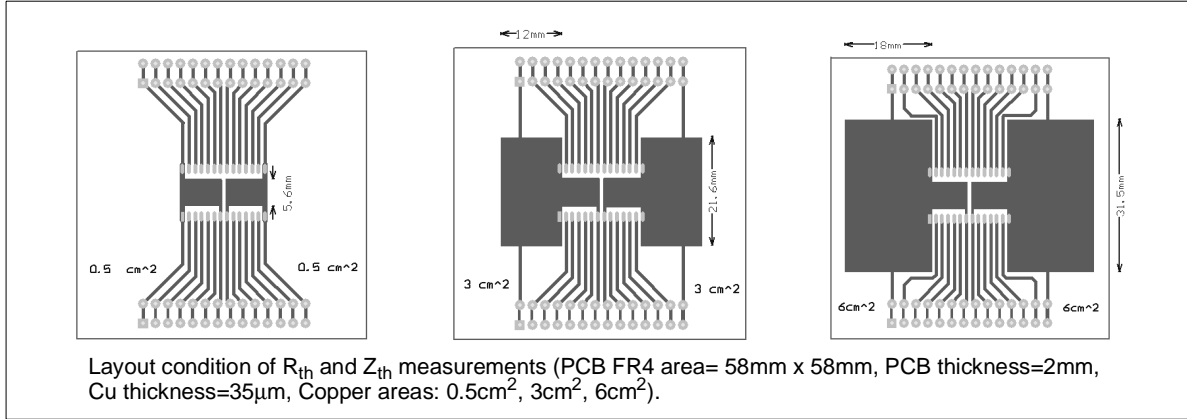
Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



**SO-28 DOUBLE ISLAND THERMAL DATA**

**SO-28 Double island PC Board**

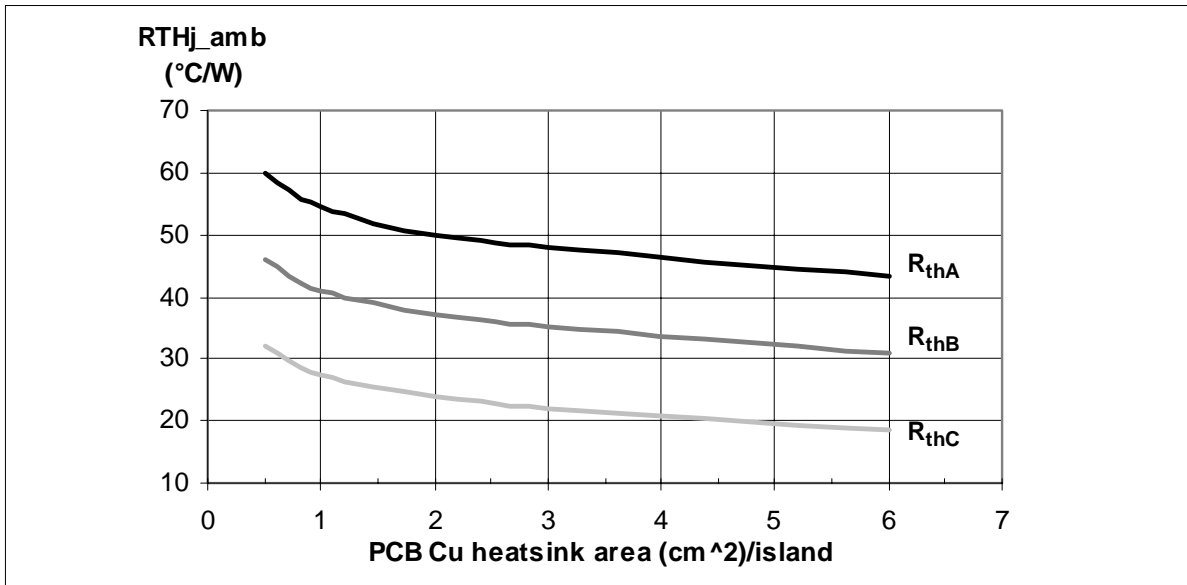


**Thermal calculation according to the PCB heatsink area**

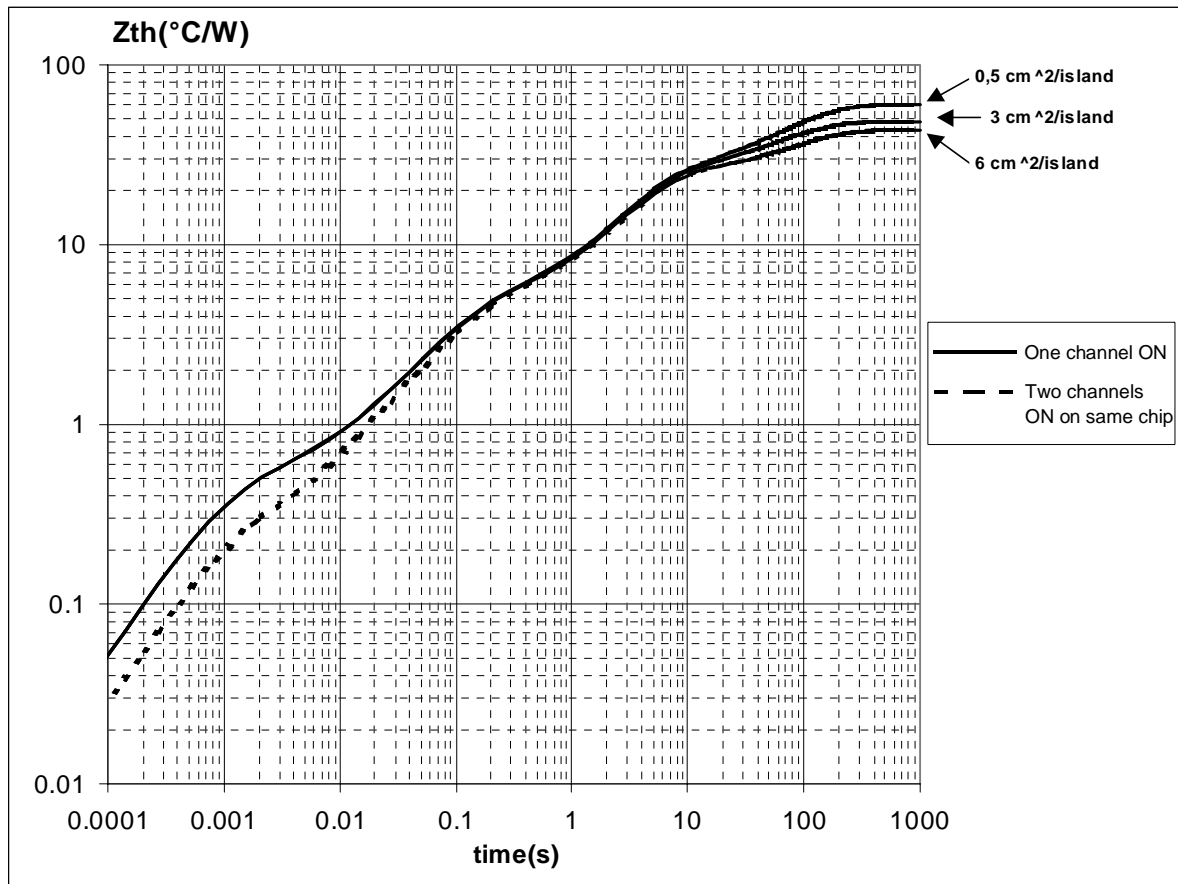
| Chip 1 | Chip 2 | $T_{jchip1}$  | $T_{jchip2}$  | Note                         |
|--------|--------|---|---|------------------------------|
| ON     | OFF    | $R_{thA} \times P_{dchip1} + T_{amb}$                               | $R_{thC} \times P_{dchip1} + T_{amb}$                               |                              |
| OFF    | ON     | $R_{thC} \times P_{dchip2} + T_{amb}$                               | $R_{thA} \times P_{dchip2} + T_{amb}$                               |                              |
| ON     | ON     | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$                | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$                | $P_{dchip1} = P_{dchip2}$    |
| ON     | ON     | $(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$ | $(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$ | $P_{dchip1} \neq P_{dchip2}$ |

$R_{thA}$  = Thermal resistance Junction to Ambient with one chip ON  
 $R_{thB}$  = Thermal resistance Junction to Ambient with both chips ON and  $P_{dchip1} = P_{dchip2}$   
 $R_{thC}$  = Mutual thermal resistance

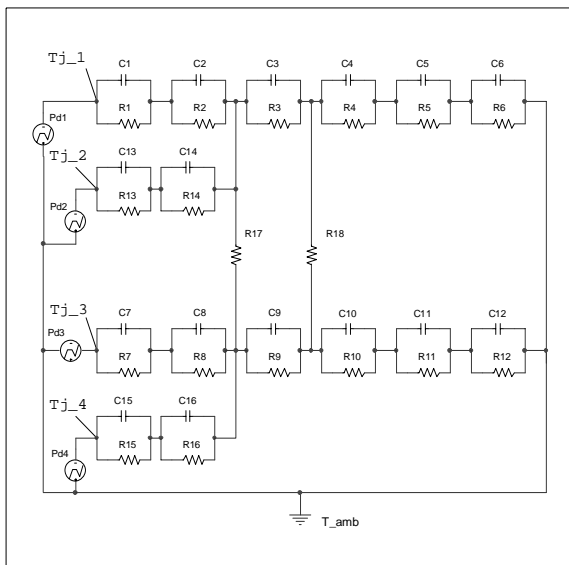
**$R_{thj-amb}$  Vs. PCB copper area in open box free air condition**



SO-28 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a four channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THip}(1 - \delta)$$

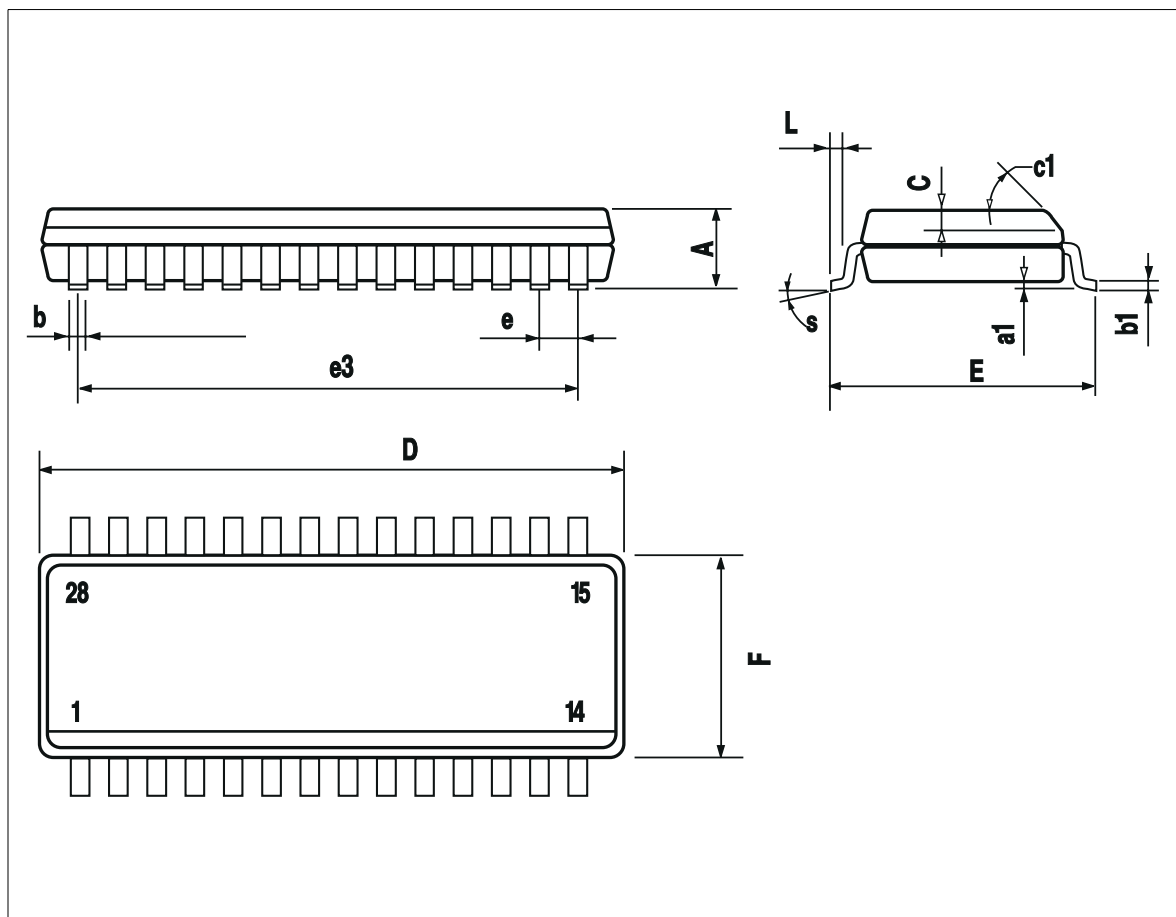
where  $\delta = t_p/T$

Thermal Parameter

| Area/island (cm <sup>2</sup> ) | 0.5      | 6  |
|--------------------------------|----------|----|
| R1=R7=R13=R15 (°C/W)           | 0.05     |    |
| R2=R8=R14=R16 (°C/W)           | 0.3      |    |
| R3=R9 (°C/W)                   | 3.4      |    |
| R4=R10 (°C/W)                  | 11       |    |
| R5=R11 (°C/W)                  | 15       |    |
| R6=R12 (°C/W)                  | 30       | 13 |
| C1=C7=C13=C15 (W.s/°C)         | 0.001    |    |
| C2=C8=C14=C16 (W.s/°C)         | 5.00E-03 |    |
| C3=C9 (W.s/°C)                 | 1.00E-02 |    |
| C4=C10 (W.s/°C)                | 0.2      |    |
| C5=C11 (W.s/°C)                | 1.5      |    |
| C6=C12 (W.s/°C)                | 5        | 8  |
| R17=R18 (°C/W)                 | 150      |    |

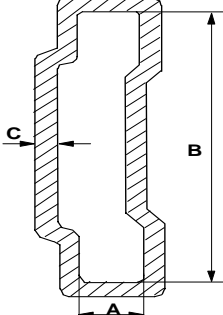
**SO-28 MECHANICAL DATA**

| DIM. | mm.       |       |       | inch  |       |       |
|------|-----------|-------|-------|-------|-------|-------|
|      | MIN.      | TYP   | MAX.  | MIN.  | TYP.  | MAX.  |
| A    |           |       | 2.65  |       |       | 0.104 |
| a1   | 0.10      |       | 0.30  | 0.004 |       | 0.012 |
| b    | 0.35      |       | 0.49  | 0.013 |       | 0.019 |
| b1   | 0.23      |       | 0.32  | 0.009 |       | 0.012 |
| C    |           | 0.50  |       |       | 0.020 |       |
| c1   | 45 (typ.) |       |       |       |       |       |
| D    | 17.7      |       | 18.1  | 0.697 |       | 0.713 |
| E    | 10.00     |       | 10.65 | 0.393 |       | 0.419 |
| e    |           | 1.27  |       |       | 0.050 |       |
| e3   |           | 16.51 |       |       | 0.650 |       |
| F    | 7.40      |       | 7.60  | 0.291 |       | 0.299 |
| L    | 0.40      |       | 1.27  | 0.016 |       | 0.050 |
| S    | 8 (max.)  |       |       |       |       |       |





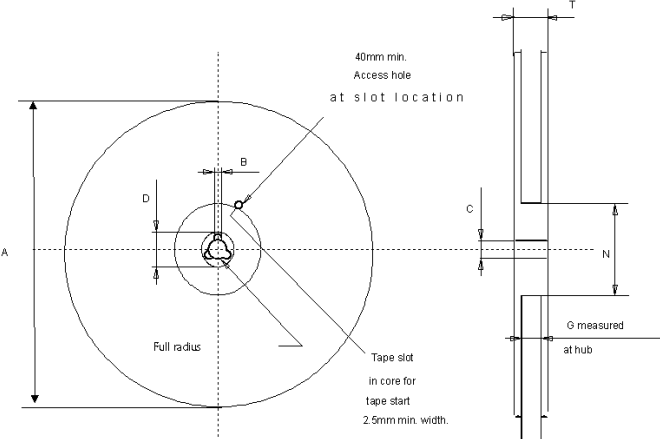
**SO-28 TUBE SHIPMENT (no suffix)**



|                            |      |
|----------------------------|------|
| <b>Base Q.ty</b>           | 28   |
| <b>Bulk Q.ty</b>           | 700  |
| <b>Tube length (± 0.5)</b> | 532  |
| <b>A</b>                   | 3.5  |
| <b>B</b>                   | 13.8 |
| <b>C (± 0.1)</b>           | 0.6  |

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**

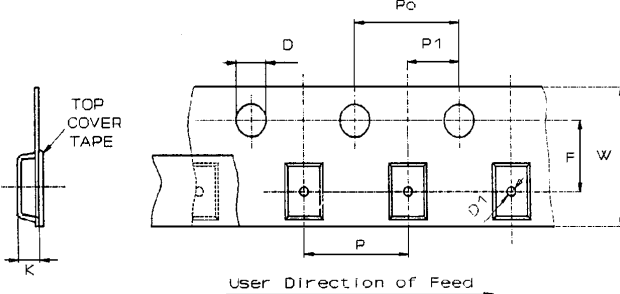


|                      |      |
|----------------------|------|
| <b>Base Q.ty</b>     | 1000 |
| <b>Bulk Q.ty</b>     | 1000 |
| <b>A (max)</b>       | 330  |
| <b>B (min)</b>       | 1.5  |
| <b>C (± 0.2)</b>     | 13   |
| <b>F</b>             | 20.2 |
| <b>G (+ 2 / - 0)</b> | 16.4 |
| <b>N (min)</b>       | 60   |
| <b>T (max)</b>       | 22.4 |

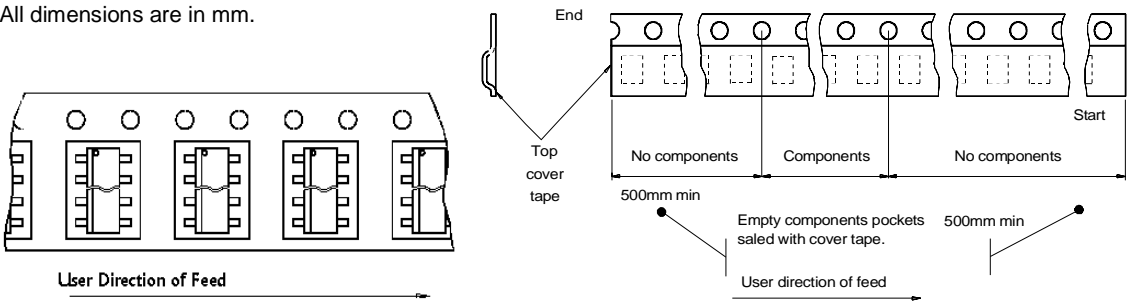
**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

|                          |                     |     |
|--------------------------|---------------------|-----|
| <b>Tape width</b>        | <b>W</b>            | 16  |
| <b>Tape Hole Spacing</b> | <b>P0 (± 0.1)</b>   | 4   |
| <b>Component Spacing</b> | <b>P</b>            | 12  |
| <b>Hole Diameter</b>     | <b>D (± 0.1/-0)</b> | 1.5 |
| <b>Hole Diameter</b>     | <b>D1 (min)</b>     | 1.5 |
| <b>Hole Position</b>     | <b>F (± 0.05)</b>   | 7.5 |
| <b>Compartment Depth</b> | <b>K (max)</b>      | 6.5 |
| <b>Hole Spacing</b>      | <b>P1 (± 0.1)</b>   | 2   |



All dimensions are in mm.



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